CLAIMS

What is claimed is:

1. A method for interleaving data elements comprising the steps of:

writing address locations of the data elements sequentially by rows into a matrix having a predetermined number of bit storage locations arranged in a first predetermined number of rows having corresponding row indexes and a second predetermined number of columns having corresponding column indexes;

bit reversing the row indexes for the first predetermined number of rows and permuting the corresponding address locations of the data elements;

bit reversing the column indexes for the second predetermined number of columns and permuting the corresponding address locations of the data elements; and

shifting bit storage locations of one or more of the first predetermined number of rows a respective predetermined number of columns.

2. The method according to claim 1, further comprising the steps of:

determining an N number of bits within a frame to be transmitted and setting the predetermined number of bit storage locations equal to N; and

setting the first predetermined number of rows and second predetermined number of columns to 2^m and 2^n, respectively, where the values m and n are set such that 2^{n+m} is greater than or equal to N.

3. The method according to claim 2, wherein the values of m and n are set such that n is greater than or equal to m and that the absolute value of the difference of values m and n is less than or equal to one.

4. The method according to claim 1, further comprising the step of reading the data elements out of the matrix column by column starting with a first column after the columns have been reversed and the rows have been reversed and shifted.

5. The method according to claim 1, wherein the steps of reversing bit storage locations for the first predetermined number of rows, reversing bit storage locations for the second predetermined number of columns, and shifting bit storage locations of each of the second predetermined number of rows a respective predetermined number of columns are performed for each data element when each individual data element is written to the matrix.

6. The method according to claim 2, wherein data elements in each particular row of the matrix are each shifted in a predetermined direction within the matrix a specified number of columns as determined by the relationship 2^m - (row# - 1), where row# is a number of the particular row in the matrix and 2^m is the total number of rows in the matrix.

7. An interleaver comprising:

a input device configured for receiving and temporarily storing data elements in an input memory, the input device also configured to write addresses of the elements in the input memory sequentially by rows into a matrix of at least a predetermined number of bit storage locations having a first predetermined number of rows and a second predetermined number of columns;

a controller configured to bit reverse row indexes for the first predetermined number of rows and permute the corresponding data elements, bit reverse column indexes for the second predetermined number of columns and permute the corresponding data elements, and shift bit storage locations of one or more of the first predetermined number of rows a respective predetermined number of columns; and

an output device configured to sequentially read the interleaved input memory addresses from the columns of the matrix and read and transmit data elements stored at corresponding memory addresses in the sequential read order of the interleaved input memory addresses.

8. The interleaver according to claim 7, wherein the controller is further configured to:

determine an N number of bits within a frame to be transmitted;

set the predetermined number of bit storage locations equal to N; and

set the first predetermined number of rows and second predetermined number of columns to 2^m and 2^n, respectively, where the values m and n are set such that 2^{n+m} is greater than or equal to the at least N number of bit storage locations.

9. The interleaver according to claim 8, wherein the values of m and n are set such that n is greater than or equal to m and that the absolute value of the difference of values m and n is less than or equal to one.

10. The interleaver according to claim 7, wherein the output device sequentially reads the data elements out of the matrix column by column starting with a first column.

11. The interleaver according to claim 7, wherein the controller is configured to reverse the bit storage locations for the first predetermined number of rows, reverse the bit storage locations for the second predetermined number of columns, and shift the bit storage locations of each of the second predetermined number of rows a respective predetermined number of columns for each data element when each individual data element is written to the matrix.

12. The interleaver according to claim 7, wherein the controller is configured to shift data elements in each particular row of the matrix a predetermined direction within the matrix a specified number of columns as determined by the relationship 2^m - (row#-1), where row# is a number of the particular row in the matrix and 2^m is the total number of rows in the matrix.

13. A data transmission system employing turbo encoding comprising:

a turbo encoder for turbo encoding received data frames and transmitting the encoded data frames within the data transmission system, the turbo encoder including:

a plurality of coders for coding the received data frame; and

an interleaver located between an input to the turbo encoder and one of the plurality of coder, the interleaver configured to interleave address locations of bits within a matrix having a first predetermined number of rows and a second predetermined number of columns by bit reversing row indexes for the first predetermined number of rows and permuting the corresponding data elements, bit reversing column indexes for the second predetermined number of columns and permuting the corresponding data elements, and shifting bit storage locations of one or more of the first predetermined number of rows a respective predetermined number of columns; and

a decoder configured to receive and decode the turbo encoded data frames transmitted by the turbo encoder, the decoder including a de-interleaver that receives the interleaved reassembles the address locations of bits within the matrix by reversing the interleaved output of the interleaver using reverse steps of the interleaver.

14. An interleaver comprising:

an input data memory configured to store an N number of bits at corresponding input data memory addresses;

an interleaver matrix configured to read and store the input data memory addresses in at least a two-dimensional matrix having a first predetermined number of rows and a second predetermined number of columns, each of the rows and columns having an assigned index value;

a controller configured to set the first predetermined number of rows and the second predetermined number of rows based on the N number of bits using a prescribed algorithm; the controller also configured to interleave the data memory address in the interleaver matrix by bit reversing the row index values for the first predetermined number of rows and permuting the corresponding address locations of the data elements, bit reversing the column index values for the second predetermined number of columns and permuting the corresponding address locations of the data elements, and shifting bit storage locations of one or more of the first predetermined number of rows a respective predetermined number of columns; the controller further configured to read out interleaved data bit addresses in the interleaver matrix column by column to produce an interleaved output read sequence;

an output buffer receiving the interleaved output read sequence from the controller, the output buffer configured to direct the input data memory to read out data bit according to the interleaved output read sequence; and

an output data memory configured to write data bits read out from the input data memory according to the interleaved output read sequence and transmit the read bits to a communication system.

15. The interleaver according to claim 14, wherein the interleaver matrix is effected within the controller.

16. The interleaver according to claim 14, wherein the controller is further configured to set the first predetermined number of rows and second predetermined number of columns to 2^m and 2^n, respectively, where the values m and n are set such that 2^{n+m} is greater than or equal to the at least N number of bit storage locations.

17. The interleaver according to claim 16, wherein the values of m and n are set such that n is greater than or equal to m and that the absolute value of the difference of values m and n is less than or equal to one.

18. The interleaver according to claim 17, wherein the controller is configured to reverse the bit storage locations for the first predetermined number of rows, reverse the bit storage locations for the second predetermined number of columns, and shift the bit storage locations of each of the second predetermined number of rows a respective predetermined number of columns for each data element when each individual data element is written to the matrix.

19. The interleaver according to claim 14, wherein the controller is configured to shift data elements in each particular row of the matrix a predetermined direction within the matrix a specified number of columns as determined by the relationship 2^m - (row#-1), where row# is a number of the particular row in the matrix and 2^m is the total number of rows in the matrix.